REMARKS

The outstanding Action has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. By this Amendment, claim 1 is amended for editorial consideration, and new claims 16 and 17 are added to further set forth the present invention regarding an additional address space of equal width. The new claims are supported by, e.g., paragraphs 0019-0024 of the specification. No new matter is introduced. Accordingly, claims 1-17 are now pending in this application and submitted for consideration.

Priority

It is noted that the Applicant's claim for priority under 35 U.S.C. 119 and certified copy of the priority document for foreign application No. 2000-095239 were not acknowledged in the outstanding Action. Therefore, prompt acknowledgment of the priority claim and receipt of the priority document is respectfully requested.

Section 102 Rejection

Claims 12-15 are rejected under 35 U.S.C. §102(e) as being anticipated by *Knox et al.* (U.S. Patent No. 6,175,388, hereinafter "*Knox*").

This rejection, which is based on an inaccurate understanding of ***Knox***., is respectfully traversed for the reasons stated below.

Knox teaches a way to set up a storage circuit for generating OSD massages. More specifically, regarding the step of setting up a range of an image area, ***Knox***

discloses that data of images and ODS bit map data, other than image data, are stored in a memory 140 (see 3: 5-11). According to ***Knox***, an OSD bit map is defined as a set of regions of programmable position and size, and written into an OSD buffer of the memory 140 assigned by user's specifications (see 3: 29-42). When the OSD function is enabled, a processor 130 manipulates the data in the memory 140 to construct an OSD bitstream. The OSD bitstream contains an OSD header and OSD data.

Referring to the step of writing data into an additional area, ***Knox*** teaches that an OSD unit retrieves the OSD bitstream from a storage device, the OSD bitstream containing the OSD header and OSD data (see 1: 50-53). As to the step of writing image data, ***Knox*** teaches that in a decoding system 100, the processor 130 receives bitstreams 120 and 110 as its inputs (see 2: 48-55). The bitstreams 120 may comprise encoded audio and video elementary streams (see 2: 31-34), and the bitstreams 110 may comprise various control signals or other data streams not included in the bitstreams 120 (see 2: 49-51). ***Knox*** also describes that the processor 130 writes received bitstreams 120 into the memory 140 via a video (2:65-66) decoder 160. Further, with respect to the step of reading out image data, ***Knox*** discloses that the video decoder 160 and OSD unit 150 both form streams of digital words (4: 30-35).

In item 2 of the outstanding Action, it is stated that various portions of ***Knox*** teach that a bit map is configured in the memory 140 as an additional area, the OSD device obtains OSD bitstreams from the storage device, and the processor 130 supplies the memory 140 with the bitstreams 120 (image data) to write it into the memory. However, ***Knox*** simply does not teach that data are written in with the address of an

additional area, and is particularly silent with respect to writing bitstreams, which are the actual data. Therefore, ***Knox*** does not teach writing of data other than image data.

Additionally, the outstanding Action cites ***Knox*** (4: 30-35) as disclosing a video decoder 160 and OSD unit 150 forming steams or sequences of digital words. ***Knox***, however, does not particularly describe that the image data and data other than image data are read out from the memory 140. In other words, ***Knox*** does not teach the reading step as set forth in claims 12-15.

Section 103 Rejections

Claims 1, 2 and 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Sherburne* (U.S. Patent No. 5,818,433) in view of *Knierim* (U.S. Patent No. 4,755,810).

Sherburne discloses an access control circuit and an area adjustment circuit. More specifically, ***Sherburne*** teaches an image processor which includes a memory 30 functioning as a storage circuit and an input/output circuit comprising a register-decoder 38 having eight-bit output providing sixteen pixels of data obtained every five memory cycles and register-decoders 36 and 40 producing two bits of overlay data.

There is not sufficient disclosure in ***Sherburne***, even in view of ***Knierim***, which is merely directed to a screen refresh operation, to render the present invention as set forth in 1, 2 and 11 obvious. For instance, ***Sherburne*** fails to teach or suggest the operational relationship between the circuit components cited in the outstanding Action.

By comparing the claimed invention with ***Sherburne***, it is apparent that the relationship of the elements which are not explicitly described in the ***Sherburne*** is improperly used by the outstanding Action to conclude that all claimed features are disclosed by ***Sherburne***.

Additionally, the outstanding Action asserts that ***Sherburne*** teaches an address generation circuit, which is not explicitly shown by any figures of ***Sherburne***, but derived from a reference that the memory planes are simultaneously addressed with the corresponding image planes (see 2: 17-21). The outstanding Action also relied on the disclosure of ***Sherburne*** regarding data defining a pixel or a plurality of pixels dependent upon the width of the display memory are simultaneously available and clocked out pixel by pixel to define each pixel in the image in order to conclude that ***Sherburne*** discloses the access control circuit and area adjustment circuit of the claimed invention. However, it is respectfully submitted that such assertions are based on improper reading and conjecture of ***Sherburne***. Indeed, ***Sherburne*** does not have any clear description on the operative relationship between, e.g. the teaching of the prior art as described in column 2, lines 17-21, and that of the illustrative embodiment as discussed in column 4, lines 24-40.

By contrast, the access control circuit as recited in claims 1, 2 and 11 is adapted to control access of writing in and reading out image data to and from a storage circuit, and the area adjustment circuit as recited therein is adapted to set up an additional area storing therein data other than the image data to adjust the address generated by the address generation circuit.

Referring to ***Knierim***, it has no relevance to the claimed invention except for the disclosure of a screen refresh operation, which does not supplement the above-discussed deficiencies of ***Sherburne***.

Claims 3, 5-10 are rejected under 35 U.S.C. §103(a) as being unpatentable *Sherburne* in view of *Knierim* (U.S. Patent No. 4,755,810) and *Knox*.

Claims 3 and 5-10 depend from claim 1 and are therefore patentable over ***Sherburne***, ***Knierim***, and ***Knox*** for at least the reasons stated above with respect to claim 1, as amended.

Claim 4 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Sherburne* in view of *Knierim* and *Herz et al.* (U.S. Patent No. 5,883,675, hereinafter"*Herz*").

Herz is specifically cited to compensate for the acknowledged deficiency in ***Sherburne*** and ***Knierim*** regarding an area adjustment circuit setting the size of the additional area. However, since ***Herz*** also does not teach or suggest the above discussed deficiencies of ***Sherburne*** and ***Knierim***, and therefore claim 4, which depends from claim 1, is distinguishable over ***Herz*** for at least the reasons stated above with respect to claim 1.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1-17 and the prompt issuance of a Notice of Allowability are respectfully solicited.

If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, Applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300.

Respectfully submitted,

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Enclosures: Marked-Up Version of Amended Claim(s)

MARKED-UP VERSION OF AMENDED CLAIM(S)

1. (Amended) An image processor comprising:

a storage circuit storing therein image data;

a data input/output circuit controlling input/output of the image data;

an access control circuit controlling access of writing in and reading out the image data to and from said storage circuit;

a refresh circuit controlling refreshing of said storage circuit; and

a memory control circuit comprising an address generation circuit generating an address in said storage circuit to and from which the image data is written in and read out,

said memory control circuit comprising an area adjustment circuit which sets up an additional area adjacent to an area in which the image data [is] <u>are</u> actually stored in a memory space of said storage circuit and storing therein data other than the image data, which adjusts the address generated by said address generation circuit, and which reads out the image data from said storage circuit, including the data in the additional area, in response to the address and a read control signal supplied to said storage circuit.